What is claimed is:

1. A floating-gate memory cell, comprising:

a gate stack having a control-gate layer and having a floating-gate layer interposed between the control-gate layer and a first semiconductor region having a first conductivity type;

a drain region in the first semiconductor region, wherein the drain region has a second conductivity type different from the first conductivity type; and

a source region in the first semiconductor region and having the second conductivity type;

wherein the source region is coupled to a second semiconductor region underlying the first semiconductor region; and

wherein the second semiconductor region has the second conductivity type.

2. The floating-gate memory cell of claim 1, wherein the source region is coupled to the second semiconductor region through a conductive source-line contact.

3. The floating-gate memory cell of claim 2, further comprising a conductive trace coupled between the source region and the source-line contact.

4. The floating-gate memory cell of claim 3, wherein the conductive trace is formed in the first semiconductor region.

5. The floating-gate memory cell of claim 4, wherein the conductive trace is a conductively-doped region formed in the first semiconductor region and having the second conductivity type.

6. The floating-gate memory cell of claim 4, wherein the conductive trace contains a metal silicide.

7. The floating-gate memory cell of claim 3, wherein the conductive trace is formed on the first semiconductor region.

8. The floating-gate memory cell of claim 2, wherein the source-line contact comprises a columnar trench of conductive fill material.

9. The floating-gate memory cell of claim 2, wherein the source-line contact comprises an extended trench of conductive fill material and wherein the extended trench of conductive fill material is coupled to source regions of other floating-gate memory cells.

10. The floating-gate memory cell of claim 2, wherein the source-line contact comprises a conductive fill material formed on sidewalls and a bottom of a contact hole and wherein the sidewalls of the contact hole are defined by the first semiconductor region and the bottom of the contact hole is defined by an exposed portion of the second semiconductor region.

11. The floating-gate memory cell of claim 2, wherein the source-line contact comprises a conductive material and wherein the conductive material includes at least one material selected from the group consisting of an implanted conductively-doped region having the second conductivity type, a diffused conductively-doped region having the second conductivity type, conductively-doped polysilicon having the second conductivity type, a silicide, a polycide, a metal, a metal alloy, and a conductive metal oxide.

12. The floating-gate memory cell of claim 1, wherein the first conductivity type is a p-type conductivity and the second conductivity type is an n-type conductivity.

13. A floating-gate memory cell, comprising:

a gate stack having a control-gate layer and having a floating-gate layer interposed between the control-gate layer and a first semiconductor region having a first conductivity type;

a drain region in the first semiconductor region, wherein the drain region has a second conductivity type different from the first conductivity type; and

a source region in the first semiconductor region and having the second conductivity type;

wherein the first semiconductor region is enclosed in a second semiconductor region having the second conductivity type; and

wherein the source region is coupled to the second semiconductor region.

14. A floating-gate memory cell, comprising:

a gate stack having a control-gate layer and having a floating-gate layer, wherein the gate stack is overlying an upper well region and wherein the upper well region has a first conductivity type;

a drain region in the upper well region, wherein the drain region has a second conductivity type different from the first conductivity type;

a source region in the upper well region and having the second conductivity type; and

a source-line contact extending from the source region to a lower well region;

wherein the lower well region has the second conductivity type; and

wherein the upper well region is formed in the lower well region.

15. A floating-gate memory cell, comprising:

a gate stack having a control-gate layer and having a floating-gate layer, wherein the gate stack is overlying an upper well region and wherein the upper well region has a first conductivity type;

a drain region in the upper well region, wherein the drain region has a second conductivity type different from the first conductivity type;

a source region in the upper well region and having the second conductivity type;

a conductive trace coupled to the source region; and

a source-line contact extending from the conductive trace to a lower well region;

wherein the lower well region has the second conductivity type; and

wherein the upper well region is formed in the lower well region.

16. A floating-gate memory cell, comprising:

a tunnel dielectric layer overlying an upper well region, wherein the upper well region has a first conductivity type;

a floating-gate layer overlying the tunnel dielectric layer;

an intergate dielectric layer overlying the floating-gate layer;

a control-gate layer overlying the intergate dielectric layer;

a drain region in the upper well region, wherein the drain region has a second conductivity type different from the first conductivity type; and

a source region in the upper well region and having the second conductivity type, wherein the source region is coupled to a lower well region underlying the upper well region and having the second conductivity type.

17. The floating-gate memory cell of claim 16, wherein the tunnel dielectric layer is overlying and in contact with the upper well region, wherein the floating-gate layer is overlying and in contact with the tunnel dielectric layer, wherein the intergate dielectric layer is overlying and in contact with the floating-gate layer, and wherein the control-gate layer is overlying and in contact with the intergate dielectric layer.

18. The floating-gate memory cell of claim 16, wherein the source region is coupled to the lower well region through a conductive source-line contact.

19. The floating-gate memory cell of claim 18, further comprising a conductive trace coupled between the source region and the conductive source-line contact.

20. The floating-gate memory cell of claim 18, wherein the source-line contact comprises a columnar trench of conductive fill material.

21. The floating-gate memory cell of claim 20, wherein the source-line contact is coupled to source regions of other floating-gate memory cells.

22. The floating-gate memory cell of claim 18, wherein the source-line contact comprises an extended trench of conductive fill material and wherein the extended trench of conductive fill material is coupled to source regions of other floating-gate memory cells.

23. The floating-gate memory cell of claim 18, wherein the source-line contact comprises a conductive fill material formed on sidewalls and a bottom of a contact hole and wherein the sidewalls of the contact hole are defined by the upper well region and the bottom of the contact hole is defined by an exposed portion of the lower well region.

24. The floating-gate memory cell of claim 18, wherein the source-line contact comprises a conductive material and wherein the conductive material includes at least one material selected from the group consisting of an implanted conductively-doped region having the second conductivity type, a diffused conductively-doped region having the second conductivity type, conductively-doped polysilicon having the second conductivity type, a silicide, a polycide, a metal, a metal alloy, and a conductive metal oxide.

25. A memory device, comprising:

a substrate having a first conductivity type;

a lower well region in the substrate, wherein the lower well region has a second conductivity type different from the first conductivity type;

an upper well region in the lower well region, wherein the upper well region has the first conductivity type;

a plurality of word lines;

a plurality of bit lines; and

a plurality of floating-gate memory cells, wherein each floating-gate memory cell comprises:

a control-gate layer for coupling to one of the plurality of word lines;

a floating-gate layer interposed between the control-gate layer and the upper well region;

a drain region in the upper well region for coupling to one of the plurality of bit lines, wherein the drain region has the second conductivity type;

a source region in the upper well region, wherein the source region has the second conductivity type; and

a source-line contact extending below the source region to the lower well region and providing electrical communication between the source region and the lower well region.

26. The memory device of claim 25, wherein each source-line contact is laterally displaced from each source region and wherein each source-line contact is coupled to at least one source region.

27. The memory device of claim 26, wherein each source-line contact is coupled to the at least one source region through a conductive trace.

28. The memory device of claim 25, wherein each source-line contact extends through at least one source region.

29. The memory device of claim 28, wherein each source-line contact extends through only one source region.

30. The memory device of claim 25, wherein each floating-gate memory cell having a control-gate layer coupled to the same word line also shares the same source-line contact.

31. A memory device, comprising:

a substrate having a first conductivity type;

a lower well region in the substrate, wherein the lower well region has a second conductivity type different from the first conductivity type;

an upper well region in the lower well region, wherein the upper well region has the first conductivity type;

a plurality of word lines;

a plurality of bit lines; and

a plurality of floating-gate memory cells, wherein each floating-gate memory cell comprises:

a control-gate layer for coupling to one of the plurality of word lines;

a floating-gate layer interposed between the control-gate layer and the upper well region;

a drain region in the upper well region for coupling to one of the plurality of bit lines, wherein the drain region has the second conductivity type;

a source region in the upper well region, wherein the source region has the second conductivity type; and

a source-line contact extending from the source region to the lower well region.

32. A memory device, comprising:

a substrate having a first conductivity type;

a first well region, wherein the first well region has the first conductivity type;

a second well region interposed between the substrate and the first well region, wherein the second well region has a second conductivity type different from the first conductivity type;

a plurality of word lines;

a plurality of bit lines; and

a plurality of floating-gate memory cells, wherein each floating-gate memory cell comprises:

a control-gate layer for coupling to one of the plurality of word lines;

a floating-gate layer interposed between the control-gate layer and the first well region;

a drain region in the first well region for coupling to one of the plurality of bit lines, wherein the drain region has the second conductivity type;

a source region in the first well region, wherein the source region has the second conductivity type; and

a source-line contact extending below the source region to the second well region and providing electrical communication between the source region and the second well region.

33. A memory device, comprising:

a substrate having a first conductivity type;

a first well region, wherein the first well region has the first conductivity type;

a second well region interposed between the substrate and the first well region, wherein the second well region has a second conductivity type different from the first conductivity type;

a third well region, wherein the third well region has the first conductivity type and wherein the third well region is isolated from the first well region;

a fourth well region interposed between the substrate and the third well region, wherein the fourth well region has the second conductivity type;

a first plurality of word lines;

a second plurality of word lines;

a plurality of bit lines;

a first block of floating-gate memory cells of a memory array, wherein each floating-gate memory cell of the first block of floating-gate memory cells comprises:

a control-gate layer for coupling to one of the first plurality of word lines;

a floating-gate layer interposed between the control-gate layer and the first well region;

a drain region in the first well region for coupling to one of the plurality of bit lines, wherein the drain region has the second conductivity type;

a source region in the first well region, wherein the source region has the second conductivity type; and

a source-line contact extending below the source region to the second well region and providing electrical communication between the source region and the second well region; and

a second block of floating-gate memory cells of the memory array, wherein each floating-gate memory cell of the second block of floating-gate memory cells comprises:

a control-gate layer for coupling to one of the second plurality of word lines;

a floating-gate layer interposed between the control-gate layer and the third well region;

a drain region in the third well region for coupling to one of the plurality of bit lines, wherein the drain region has the second conductivity type;

a source region in the third well region, wherein the source region has the second conductivity type; and

a source-line contact extending below the source region to the fourth well region and providing electrical communication between the source region and the fourth well region.

34. The memory device of claim 33, wherein the second well region and the fourth well region are the same well region.

35. The memory device of claim 33, wherein each control-gate layer coupled to each word line of the first plurality of word lines is associated with a floating-gate memory cell of the first block of floating-gate memory cells.

36. The memory device of claim 33, wherein each source-line contact is laterally displaced from each source region and wherein each source-line contact is coupled to at least one source region.

37. The memory device of claim 36, wherein each source-line contact is coupled to the at least one source region through a conductive trace.

38. The memory device of claim 33, wherein each source-line contact extends through at least one source region.

39. The memory device of claim 38, wherein each source-line contact extends through only one source region.

40. The memory device of claim 33, wherein each floating-gate memory cell having a control-gate layer coupled to the same word line also shares the same source-line contact.

41. A floating-gate memory cell, comprising:

a gate stack having a control-gate layer and having a floating-gate layer interposed between the control-gate layer and a well region having a first conductivity type, wherein the well region having the first conductivity type is isolated from a semiconductor substrate having the first conductivity type by an interposing well region having a second conductivity type different from the first conductivity type;

a first source/drain region having the second conductivity type in the well region having the first conductivity type; and

a second source/drain region having the second conductivity type in the well region having the first conductivity type, wherein the second source/drain region is coupled to the well region having the second conductivity type.

42. The floating-gate memory cell of claim 41, wherein the well region having the first conductivity type is a p-well and wherein the interposing well region having the second conductivity type is an n-well in a p-type semiconductor substrate.

43. The floating-gate memory cell of claim 41, wherein the well region having the first conductivity type is an n-well and wherein the interposing well region having the second conductivity type is a p-well in an n-type semiconductor substrate.

44. A floating-gate memory cell, comprising:

a gate stack having a control-gate layer and having a floating-gate layer interposed between the control-gate layer and a p-well, wherein the p-well is enclosed in an n-well formed in a p-type semiconductor substrate;

a drain region in the p-well, wherein the drain region has an n^+-type conductivity; and

a source region in the p-well and having the n^+-type conductivity, wherein the source region is coupled to the n-well.

45. A floating-gate memory cell, comprising:

a gate stack having a control-gate layer and having a floating-gate layer, wherein the gate stack is overlying a p-well and wherein the p-well is enclosed in an n-well formed in a p-type semiconductor substrate;

an n^+-type drain region in the p-well;

an n^+-type source region in the p-well; and

a source-line contact coupled to the n^+-type source region and extending below the n^+-type source region to the n-well.

46. A floating-gate memory cell, comprising:

a gate stack having a control-gate layer and having a floating-gate layer, wherein the gate stack is overlying a p-well and wherein the p-well is enclosed in an n-well formed in a p-type semiconductor substrate;

an n^+-type drain region in the p-well;

an n^+-type source region in the p-well; and

a source-line contact extending from the n^+-type source region to the n-well.

47. The floating-gate memory cell of claim 46, wherein the source-line contact extends from multiple n^+-type source regions to the n-well.

48. The floating-gate memory cell of claim 46, wherein the source-line contact extends from only one n^+-type source region to the n-well.

49. A floating-gate memory cell, comprising:

a gate stack having a control-gate layer and having a floating-gate layer, wherein the gate stack is overlying a p-well and wherein the p-well is enclosed in an n-well formed in a p-type semiconductor substrate;

an n^+-type drain region in the p-well;

an n^+-type source region in the p-well;

a source-line contact extending below the n^+-type source region to the n-well; and

a conductive trace in the p-well and coupled between the n^+-type source region and the source-line contact.

50. The floating-gate memory cell of claim 49, wherein the conductive trace is further coupled between at least one additional n^+-type source region and the source-line contact.

51. The floating-gate memory cell of claim 49, wherein the conductive trace is further coupled to at least one additional source-line contact.

52. The floating-gate memory cell of claim 49, wherein the conductive trace contains a conductive material selected from the group consisting of a conductively-doped silicon-containing material and a metal silicide.

53. A floating-gate memory cell, comprising:

a gate stack having a control-gate layer and having a floating-gate layer, wherein the gate stack is overlying a p-well and wherein the p-well is enclosed in an n-well formed in a p-type semiconductor substrate;

an n^+-type drain region in the p-well;

an n^+-type source region in the p-well;

a source-line contact extending below the n^+-type source region to the n-well; and

an n^+-type conductive trace in the p-well and coupled between the n^+-type source region and the source-line contact.

54. A floating-gate memory cell, comprising:

a tunnel dielectric layer overlying an upper well region, wherein the upper well region has a p-type conductivity;

a floating-gate layer overlying the tunnel dielectric layer;

an intergate dielectric layer overlying the floating-gate layer;

a control-gate layer overlying the intergate dielectric layer;

a drain region in the upper well region, wherein the drain region has an n^+-type conductivity; and

a source region in the upper well region and having the n^+-type conductivity, wherein the source region is coupled to a lower well region underlying the upper well region;

wherein the lower well region has an n-type conductivity; and

wherein the lower well region is formed in a semiconductor substrate having the p-type conductivity.

55. The floating-gate memory cell of claim 54, wherein the source region is coupled to the lower well region through a source-line contact as a columnar trench of conductive fill material.

56. The floating-gate memory cell of claim 55, further comprising a conductive trace coupled between the source region and the source-line contact.

57. The floating-gate memory cell of claim 54, wherein the source region is coupled to the lower well region through a source-line contact as an extended trench of conductive fill material and wherein the extended trench of conductive fill material is coupled to source regions of other floating-gate memory cells.

58. A memory device, comprising:

a substrate having a p-type conductivity;

a lower well region formed in the substrate, wherein the lower well region has an n-type conductivity;

an upper well region formed in the lower well region, wherein the upper well region has the p-type conductivity;

a plurality of word lines;

a plurality of bit lines; and

a plurality of floating-gate memory cells, wherein each floating-gate memory cell comprises:

a control-gate layer for coupling to one of the plurality of word lines;

a floating-gate layer interposed between the control-gate layer and the upper well region;

a drain region in the upper well region for coupling to one of the plurality of bit lines, wherein the drain region has an n^+-type conductivity;

a source region in the upper well region, wherein the source region has the n^+-type conductivity; and

a source-line contact extending below the source region to the lower well region, wherein the source-line contact is coupled to the source region.

59. The memory device of claim 58, wherein each source-line contact is laterally displaced from each source region and wherein each source-line contact is coupled to at least one source region.

60. The memory device of claim 59, wherein each source-line contact is coupled to the at least one source region through a conductive trace.

61. The memory device of claim 58, wherein each source-line contact extends through at least one source region.

62. The memory device of claim 61, wherein each source-line contact extends through only one source region.

63. The memory device of claim 58, wherein each floating-gate memory cell having a control-gate layer coupled to the same word line also shares the same source-line contact.

64. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes

an array of floating-gate memory cells arranged in rows and columns with word lines coupled to rows of floating-gate memory cells and bit lines coupled to columns of floating-gate memory cells, and wherein at least one of the floating-gate memory cells comprises:

a gate stack having a control-gate layer coupled to a word line and having a floating-gate layer interposed between the control-gate layer and a first semiconductor region having a first conductivity type;

a drain region in the first semiconductor region coupled to a bit line, wherein the drain region has a second conductivity type different from the first conductivity type; and

a source region in the first semiconductor region and having the second conductivity type;

wherein the source region is coupled to a second semiconductor region underlying the first semiconductor region; and

wherein the second semiconductor region has the second conductivity type.

65. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device comprises:

a substrate having a first conductivity type;

a lower well region in the substrate, wherein the lower well region has a second conductivity type different from the first conductivity type;

an upper well region in the lower well region, wherein the upper well region has the first conductivity type;

a plurality of word lines;

a plurality of bit lines;

an array of floating-gate memory cells, wherein each floating-gate memory cell comprises:

a control-gate layer for coupling to one of the plurality of word lines;

a floating-gate layer interposed between the control-gate layer and the upper well region;

a drain region in the upper well region for coupling to one of the plurality of bit lines, wherein the drain region has the second conductivity type;

a source region in the upper well region, wherein the source region has the second conductivity type; and

a source-line contact extending below the source region to the lower well region, wherein the source-line contact is coupled to the source region; and

a plurality of data lines coupled between the array of floating-gate memory cells and the processor.

66. A method of reading a floating-gate memory cell, comprising:

applying a first potential to a control gate of the floating-gate memory cell, wherein the first potential is greater than a threshold voltage of the

memory cell in a first programmed state and less than a threshold voltage of the memory cell in a second programmed state, wherein the floating-gate memory cell has a drain region and a source region in a first well region having a first conductivity type, and wherein the first well region is in a second well region having a second conductivity type different from the first conductivity type;

applying a second potential to the second well region, wherein the second well region is coupled to the source region;

applying a precharge potential to a bit line coupled to the drain region; and

sensing a current between the drain region and the source region after isolating the bit line from the precharge potential and while the second potential is applied to the second well region, wherein a level of the current is indicative of the programmed state of the memory cell.

67. The method of claim 66, wherein the first conductivity type is a p-type and the second conductivity type is an n-type.

68. The method of claim 66, wherein the precharge potential is a supply potential and the second potential is a ground potential.

69. The method of claim 66, wherein the second well region is an n-type well region formed in a p-type semiconductor substrate and the first well region is a p-type well region formed in the n-type well region.

70. The method of claim 66, wherein the second well region is an n-type well region formed in a p-type semiconductor substrate through controlled-depth dopant implantation and the first well region is a p-type well region defined during the controlled-depth dopant implantation.

71. The method of claim 66, wherein the method is performed in the order presented.

72. A method of programming a floating-gate memory cell, comprising:
applying a first potential to a control gate of the floating-gate memory cell, wherein the floating-gate memory cell has a drain region and a source region in a first well region having a first conductivity type, and wherein the first well region is in a second well region having a second conductivity type different from the first conductivity type;
applying a second potential to the drain region; and
applying a third potential to the second well region, wherein the second well region is coupled to the source region.

73. The method of claim 72, wherein the first conductivity type is a p-type and the second conductivity type is an n-type.

74. The method of claim 72, wherein the first potential is higher than the second potential and the second potential is higher than the third potential.

75. The method of claim 72, wherein the first potential is a first positive potential, the second potential is a second positive potential lower than the first positive potential, and the third potential is a ground potential.

76. The method of claim 72, wherein the method is performed in the order presented.

77. A method of erasing a floating-gate memory cell, comprising:
applying a first potential to a control gate of the floating-gate memory cell, wherein the floating-gate memory cell has a drain region and a source region in a first well region having a first conductivity type, and wherein

the first well region is in a second well region having a second conductivity type different from the first conductivity type; and

applying a second potential to the first well region and the second well region, wherein the second potential is higher than the first potential and wherein the second well region is coupled to the source region.

78. The method of claim 77, wherein the first conductivity type is a p-type and the second conductivity type is an n-type.

79. The method of claim 77, further comprising:
electrically floating the drain region.

80. The method of claim 77, wherein the second potential is a positive potential and the first potential is a negative potential.

81. The method of claim 77, wherein the method is performed in the order presented.

82. A method of erasing a floating-gate memory cell, comprising:
applying a first potential to a control gate of the floating-gate memory cell, wherein the floating-gate memory cell has a drain region and a source region in a first well region having a first conductivity type, and wherein the first well region is in a second well region having a second conductivity type different from the first conductivity type;

applying a second potential to the first well region, wherein the second potential is higher than the first potential; and

electrically floating the second well region, wherein the second well region is coupled to the source region.

83. The method of claim 82, wherein the first conductivity type is a p-type and the second conductivity type is an n-type.

84. The method of claim 82, further comprising:
electrically floating the drain region.

85. The method of claim 82, wherein the second potential is a positive potential and the first potential is a negative potential.

86. The method of claim 82, wherein the method is performed in the order presented.

87. A method of erasing a floating-gate memory cell, comprising:
applying a first potential to a control gate of the floating-gate memory cell, wherein the floating-gate memory cell has a drain region and a source region in a first well region having a first conductivity type, and wherein the first well region is in a second well region having a second conductivity type different from the first conductivity type;
applying a second potential to the first well region, wherein the second potential is higher than the first potential; and
electrically floating the second well region and the drain region, wherein the second well region is coupled to the source region.

88. The method of claim 87, wherein the method is performed in the order presented.

89. A method of forming a memory cell, comprising:
forming a gate stack on a first semiconductor region having a first conductivity type, wherein the first semiconductor region is enclosed in a second

semiconductor region having a second conductivity type different from the first conductivity type;

forming source/drain regions on opposing sides of the gate stack, wherein the source/drain regions have the second conductivity type; and

forming a source-line contact, wherein the source-line contact is coupled between a first source/drain region and the second semiconductor region.

90. The method of claim 89, wherein the method is performed in the order presented.

91. A method of forming a memory cell, comprising:

forming a gate stack on a first semiconductor region having a first conductivity type, wherein the first semiconductor region is enclosed in a second semiconductor region having a second conductivity type different from the first conductivity type;

forming source/drain regions on opposing sides of the gate stack, wherein the source/drain regions have the second conductivity type;

forming a conductive trace coupled to a first source/drain region; and

forming a source-line contact, wherein the source-line contact is coupled between the conductive trace and the second semiconductor region.

92. The method of claim 91, wherein the conductive trace has the second conductivity type and wherein forming the source/drain regions and forming the conductive trace occur concurrently.

93. The method of claim 91, wherein forming a source-line contact further comprises forming a columnar trench of conductive fill material.

94. The method of claim 91, wherein forming a source-line contact further comprises forming an extended trench of conductive fill material and wherein

the extended trench of conductive fill material is coupled to source regions of other floating-gate memory cells.

95. The method of claim 91, wherein forming a source-line contact further comprises forming a conductive fill material on sidewalls and a bottom of a contact hole and wherein the sidewalls of the contact hole are defined by the first semiconductor region and the bottom of the contact hole is defined by an exposed portion of the second semiconductor region.

96. The method of claim 91, wherein forming a source-line contact further comprises filling a trench with a conductive material and wherein the conductive material includes at least one material selected from the group consisting of an implanted conductively-doped region having the second conductivity type, a diffused conductively-doped region having the second conductivity type, conductively-doped polysilicon having the second conductivity type, a silicide, a polycide, a metal, a metal alloy, and a conductive metal oxide.

97. The method of claim 91, wherein the method is performed in the order presented.

98. A method of forming a memory array, comprising:

forming a plurality of gate stacks on a first semiconductor region having a first conductivity type, wherein the first semiconductor region is enclosed in a second semiconductor region having a second conductivity type different from the first conductivity type;

forming source regions in the first semiconductor region and on a first side of each gate stack, wherein the source regions have the second conductivity type;

forming drain regions in the first semiconductor region and on a second side of each gate stack, wherein the drain regions have the second conductivity type; and

forming a plurality of source-line contacts, wherein each source-line contact is coupled between the second semiconductor region and at least one source region.

99. The method of claim 98, further comprising forming a plurality of conductive traces, wherein each conductive trace couples at least one source region to a source-line contact.

100. The method of claim 98, wherein each source-line contact is coupled between the second semiconductor region and only one source region.

101. The method of claim 98, wherein each source-line contact extends through at least one source region.

102. The method of claim 98, wherein the method is performed in the order presented.

103. A method of forming a memory array, comprising:

forming a plurality of gate stacks on a p-well, wherein the p-well is isolated from a p-type substrate by an n-well;

forming n^+-type source regions in the p-well and on a first side of each gate stack;

forming n^+-type drain regions in the p-well and on a second side of each gate stack; and

forming a plurality of source-line contacts, wherein each source-line contact is coupled between the n-well and at least one n^+-type source region.

104. The method of claim 103, wherein the method is performed in the order presented.

105. A method of forming a memory array, comprising:

forming a plurality of gate stacks on a p-well, wherein the p-well is isolated from a p-type substrate by an n-well;

forming a plurality of n^+-type source regions in the p-well and on a first side of each gate stack;

forming a plurality of n^+-type drain regions in the p-well and on a second side of each gate stack;

forming a plurality of n^+-type conductive traces in the p-well, wherein each n^+-type conductive trace is coupled to multiple n^+-type source regions; and

forming a plurality of source-line contacts, wherein each source-line contact extends through an n^+-type conductive trace to the n-well.

106. The method of claim 105, wherein forming a plurality of n^+-type source regions, forming a plurality of n^+-type drain regions and forming a plurality of n^+-type conductive traces are performed concurrently.

107. The method of claim 105, wherein each source-line contact further extends through at least one n^+-type source region.

108. The method of claim 105, wherein the method is performed in the order presented.

109. A method of forming a memory array, comprising:

forming a plurality of gate stacks on a p-well, wherein the p-well is isolated from a p-type substrate by an n-well;

forming a plurality of n^+-type source regions in the p-well and on a first side of each gate stack;

forming a plurality of n^+-type drain regions in the p-well and on a second side of each gate stack; and

forming a plurality of source-line contacts, wherein each source-line contact extends through at least one n^+-type source region to the n-well.

110. The method of claim 109, wherein the method is performed in the order presented.